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**APPLICATION NOTE**

**AP-28**

# Intel® MULTIBUS™ Interfacing

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## Related Intel Publications

*INTELLEC Microcomputer Development System Hardware Reference Manual*, 98-132.

*System 80/10 Microcomputer Hardware Reference Manual*, 98-316.

*8080 Microcomputer Systems User's Manual*, 98-153.

*SBC 501 Direct Memory Access Controller Hardware Reference Manual*, 98-294.

# Intel MULTIBUS Interfacing

## Contents

## INTRODUCTION

A significant measure of the power and flexibility of the Intel OEM Computer Product Line can be attributed to the design of its system bus, the Intel MULTIBUS™. The bus structure provides a common element for communication between a wide variety of system modules which include: Single Board Computers, memory and I/O expansion boards, peripherals and controllers.

The purpose of this application note is to help you develop a basic understanding of the Intel MULTIBUS. This knowledge is essential for configuring a system containing multiple modules. Another purpose is to provide you with the information necessary to design a bus interface for a slave module. One of the tools that will be used to achieve this goal is the complete description of a general purpose slave interface. The detailed description includes a wire list that you can use to build the interface on a prototype board. Thus, you can connect your external logic to the MULTIBUS via this interface.

Other portions of this application note provide an indepth examination of the bus signals, operating characteristics (AC and DC requirements), and bus interface circuits.

## INTEL MULTIBUS

The Intel MULTIBUS includes the following signal lines: 16 address lines, 16 bidirectional data lines, and 8 multi-level interrupt lines. The address and data lines are driven by three-state devices, while the interrupt and some other control lines are open-collector driven.

Modules that use the MULTIBUS have a master-slave relationship. A bus master module can drive the command and address lines: it can control the bus. A Single Board Computer is an example of a bus master. On the other hand, a bus slave cannot control the bus. Memory and I/O expansion boards are examples of bus slaves.

Notice that a system may have a number of bus masters. Bus arbitration results when more than one master requests control of the bus at the same time. The bus clock is usually provided by one of the bus masters and is derived independently from the processor clock. The bus clock provides a timing reference for resolving bus contention among multiple requests from bus masters. For example, a processor and a DMA (direct memory access) module may both request control of the bus. This feature allows different speed masters to share resources on the same bus. Actual transfers via the bus, however, proceed asynchronously with respect to the bus clock. Thus, the transfer speed is dependent on the transmitting and receiving devices only. The bus design prevents slow master modules from being handicapped in their attempts to gain control of the bus, but does not restrict the speed at which faster modules can transfer data via the same bus. Once a bus request is granted, single or multiple read/write transfers can proceed. The most obvious applications for the master-slave capabilities of the bus are multi-processor configurations and high-speed direct-memory-access (DMA) operations. However, the master-slave capabilities of the MULTIBUS are by no means limited to these two applications.

## MULTIBUS SIGNAL DESCRIPTIONS

This section defines the signal lines that comprise the Intel MULTIBUS. Most signals on the MULTIBUS are active-low. For example, the low level of a control signal on the bus indicates active, while the low level of an address or data signal on the bus shows logic "1" value.

**NOTE**

In this application note a signal will be designated active-low by placing a slash character (/) after the mnemonic for the signal.

Appendix A contains a pin assignment list of the following signals.

### Initialization Signal Line

INIT/

*Initialization signal*; resets the entire system to a known internal state. INIT/ may be driven by one of the bus masters or by an external source such as a front panel reset switch.

### Address and Inhibit Lines

ADRØ/–ADRF/

*16 address lines*; used to transmit the address of the memory location or I/O port to be accessed. ADRF/ is the most significant bit.

INH1/

*Inhibit RAM signal*; prevents RAM memory devices from responding to the memory address on the system address bus. INH1/ effectively allows ROM memory devices to override RAM devices when ROM and RAM memory are assigned the same memory addresses. INH1/ may also be used to allow memory mapped I/O devices to override RAM memory.

INH2/

*Inhibit ROM signal*; prevents ROM memory devices from responding to the memory address on the system address bus. INH2/ effectively allows auxiliary ROM (e.g., a bootstrap program) to override ROM devices when ROM and auxiliary ROM memory are assigned the same memory addresses. INH2/ may also be used to allow memory mapped I/O devices to override ROM memory.

**Data Lines**

DATØ/–DATF/

*16 bidirectional data lines*; used to transmit or receive information to or from a memory location or I/O port. DATF/ being the most significant bit. In 8-bit systems, only lines DATØ/–DAT7/ are used (DAT7/ being the most significant bit).

**Bus Contention Resolution Lines**

BCLK/

*Bus clock*; the negative edge (high to low) of BCLK/ is used to synchronize bus contention resolution circuits. BCLK/ is asynchronous to the CPU clock. It has a 100 ns minimum period and a 35% to 65% duty cycle. BCLK/ may be slowed, stopped, or single stepped for debugging.

CCLK/

*Constant clock*; a bus signal which provides a clock signal of constant frequency for unspecified general use by modules on the system bus. CCLK/ has a minimum period of 100 ns and a 35% to 65% duty cycle.

BPRN/

*Bus priority in signal*; indicates to a particular master module that no higher priority module is requesting use of the system bus. BPRN/ is synchronized with BCLK/. This signal is not bused on the motherboard.

BPRO/

*Bus priority out signal*; used with serial (daisy chain) bus priority resolution schemes. BPRO/ is passed to the BPRN/ input of the master module with the next lower bus priority. BPRO/ is synchronized with BCLK/. This signal is not bused on the motherboard.

BUSY/

*Bus busy signal*; driven by the bus master currently in control to indicate that the bus is currently in use. BUSY/ prevents all other master modules from gaining control of the bus. BUSY/ is synchronized with BCLK/.

BREQ/

*Bus request signal*; used with parallel bus priority network to indicate that a particular master module requires use of the bus for one or more data transfers. BREQ/ is synchronized with BCLK/. This signal is not bused on the motherboard.

**Information Transfer Protocol Lines**

A bus master provides separate read/write command signals for memory and I/O devices: MRDC/, MWTC/, IORC/ and IOWC/, as explained below. When a read/write command is active, the address signals must be stabilized at all slaves on the bus. For this reason, the protocol requires that a bus master must issue address signals (and data signals if write) at least 50 ns ahead of issuing a read/write command to the bus, initiating the data transfer. The bus master must keep address signals unchanged until at least 50 ns after the read/write command is turned off, terminating the data transfer.

A bus slave must provide an acknowledge signal to the bus master in response to a read or write command signal.

MRDC/

*Memory read command*; indicates that the address of a memory location has been placed on the system address lines and specifies that the contents of the addressed location are to be read and placed on the system data bus. MRDC/ is asynchronous with BCLK/.

MWTC/

*Memory write command*; indicates that the address of a memory location has been placed on the system address lines and that a data word (8 or 16 bits) has been placed on the system data bus. MWTC/ specifies that the data word is to be written into the addressed memory location. MWTC/ is asynchronous with BCLK/.

IORC/

*I/O read command*; indicates that the address of an input port has been placed on the system address bus and that the data at that input port is to be read and placed on the system data bus. IORC/ is asynchronous with BCLK/.

IOWC/

*I/O write command*; indicates that the address of an output port has been placed on the system address bus and that the contents of the system data bus (8 or 16 bits) are to be output to the addressed port. IOWC/ is asynchronous with BCLK/.

XACK/

*Transfer acknowledge signal*; the required response of a memory location or I/O port which indicates that the specified read/write operation has been completed. That is, data has been placed on, or accepted from, the system data bus lines. XACK/ is asynchronous with BCLK/.

AACK/

*Advanced acknowledge signal*; a bus signal used as a special acknowledge signal with 8080 CPU-based systems. AACK/ is an advance acknowledge, in response to a memory read or write command. This signal allows the CPU to complete the specified operation without requiring it to wait. Interfaces which use AACK/ must also provide XACK/. This requirement must be met because not all bus masters will respond to the AACK/ signal. AACK/ is asynchronous with BCLK/.

**Asynchronous Interrupt Lines**

INTØ/–INT7/

*8 Multi-level, parallel interrupt request lines*; used with a parallel interrupt resolution network. INTØ/ has the highest priority, while INT7/ has lowest priority.

**Power Supplies**

The power supply bus pins are detailed in Appendix A which contains the pin assignment of signals on the MULTIBUS motherboard.

It is the designer's responsibility to provide adequate bulk decoupling on the board to avoid current surges on the power supply lines. It is also recommended that you provide high frequency decoupling for the logic on your board.

**Reserved**

Several bus pins are unused. However, they should be regarded as reserved for dedicated use in future Intel products.

## OPERATING CHARACTERISTICS

Beyond the definition of the MULTIBUS signals themselves it is important to examine both the AC and DC requirements of the bus. The AC requirements outline the timing of the bus signals and in particular, define the relationships between the various bus signals. On the other hand, the DC requirements specify the bus driver characteristics, maximum bus loading per board, and the pull-up/down resistors.

**AC Requirements**

The AC requirements are best presented by a discussion of the relevant timing diagrams. Table 1 contains a list of the MULTIBUS AC requirements. The most basic bus operations are those of read and write data transfers. A majority of the user designed bus interfaces will provide a slave function with direct I/O rather than memory mapped I/O or master module capability. Because of this, you may only be interested in data transfers and can therefore skip the other timing diagrams discussed in this section.

Table 1

MULTIBUS AC REQUIREMENTS

| PARAMETER | MIN. | MAX. | DESCRIPTION | REMARKS |
|---|---|---|---|---|
| $t_{BCY}$ | 100 ns | | Bus Clock Period | |
| $t_{BW}$ | 0.35 X $t_{BCY}$ | 0.65 X $t_{BCY}$ | Bus Clock Width | |
| $t_{AS}$ | 50 ns | | Address Setup Time | Relative to Active Command |
| $t_{DS}$ | 50 ns | | Write Data Setup Time | Relative to Active Command |
| $t_{AH}$ | 50 ns | | Address Hold Time | Relative to Command Removal |
| $t_{DH}$ | 50 ns | | Write Data Hold Time | Relative to Command Removal |
| $t_{DXL}$ | 0 ns | | Read Data Setup Time | Relative to Acknowledge (XACK/) |
| $t_{DXT}$ | 0 ns | | Read Data Hold Time | Relative to Command Removal |
| $t_{CX}$ | 0 ns | 100 ns | Acknowledge Hold Time | Relative to Command Removal |
| $t_{XACK}$ | 0 ns | 10 ms ▷1 | Acknowledge Delay | |
| $t_{ACC}$ | 0 ns | $t_{XACK}-t_{DXL}$ | Read Access Time | |
| $t_{CMD}$ | 100 ns | | Command Pulse Width | |
| $t_{CI}$ | | 100 ns | Inhibit Delay | Relative to Address |
| $t_{ACCB}$ | 1.5 $\mu$s ▷2 | | Acknowledge of Inhibiting slave | |

▷1 The max. is imposed only if the bus timeout feature is engaged (a field option)

▷2 $t_{ACCB}$ is a function of the cycle time of the inhibited slave

### Data Transfers

The MULTIBUS provides a maximum bandwidth of 5 MHz for single or multiple read/write transfers.

Figure 1 shows the read data transfer timing diagram.

#### *Read Data*

The address must be stable ($t_{AS}$) for a minimum of 50 ns before command. This time is typically used by the bus interface to decode the address and thus provide the required device selects. The device selects establish the data paths on the user system in anticipation of the strobe signal (command) which will follow. The minimum command pulse width is 100 ns. The address must remain stable for at least 50 ns following the command ($t_{AH}$). Valid data should not be driven onto the bus prior to command, and must not be removed until command goes away. The XACK/ signal, which is a response indicating the specified read/write operation has been completed, must coincide or follow both the read access ($t_{ACC}$) and valid data ($t_{DXL}$). XACK/ must be held until the command goes away ($t_{CX}$).

#### *Write Data*

The write data transfer timing diagram is shown in Figure 2. During a write data transfer, valid data must be presented in parallel with a stable address. Thus, the write data setup time ($t_{DS}$) has the same requirement as the address setup time ($t_{AS}$). The requirement for stable data both before and after command enables the bus interface circuitry to latch data on either the leading or trailing edge of command.

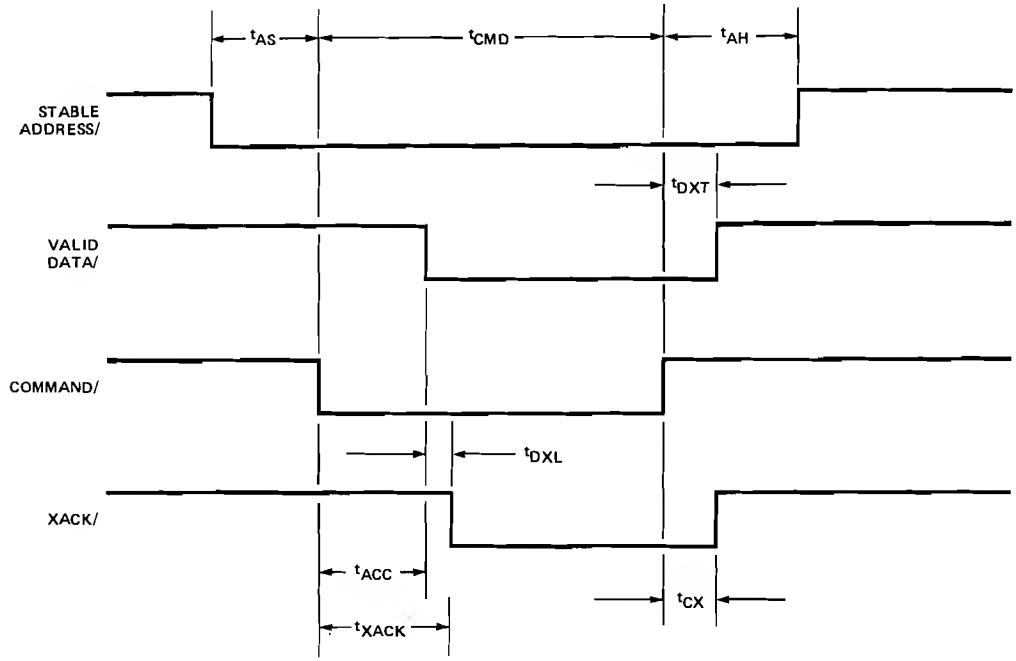



**Figure 1. Read Data Transfer**

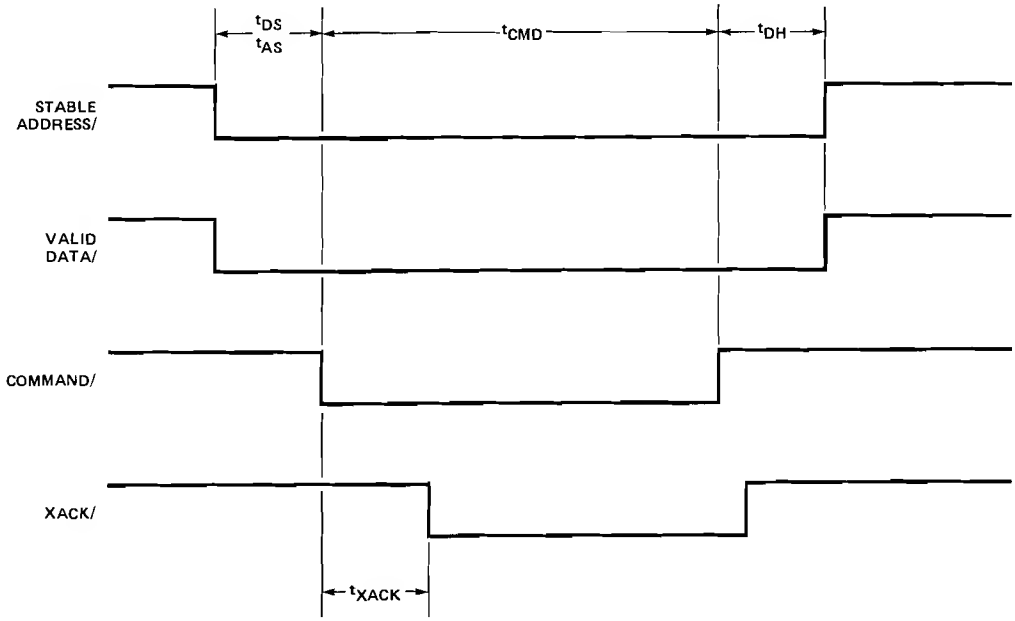



**Figure 2. Write Data Transfer**

## Inhibit Operations

Bus inhibit operations are required by certain bootstrap and memory mapped I/O configurations. The purpose of the inhibit operation is to allow a combination of RAM, ROM, or memory mapped I/O to occupy the same memory address space. In the case of a bootstrap, it may be desirable to have both ROM and RAM memory occupy the same address space, selecting ROM instead of RAM for low order memory only when the system is reset. A system designed to use memory mapped I/O, which has actual memory occupying the memory mapped I/O address space, may need to inhibit RAM or ROM memory to perform its functions.

There are two essential requirements for a successful inhibit operation. The first is that the inhibit signal must be asserted as soon as possible, within a maximum of 100 ns ($t_{CI}$), after stable address. The second requirement for a successful inhibit operation is that the acknowledge must be delayed ($t_{ACCB}$) to allow the inhibited slave to terminate any irreversible timing operations initiated by detection of a valid command prior to its inhibit.

This situation may arise because a command can be asserted within 50 ns after stable address ($t_{AS}$) and yet inhibit is not required until 100 ns ($t_{CI}$) after stable address. The acknowledge delay time ($t_{ACCB}$) is a function of the cycle time of the inhibited slave memory. Inhibiting the SBC 016 RAM board, for example, requires a minimum of 1.5 μsec. Less time is typically needed to inhibit other memory modules. For example, the SBC 104 board requires 475 ns.

Figure 3 depicts a situation in which both RAM and PROM memory have the same memory addresses. In this case PROM inhibits RAM, producing the effect of PROM overriding RAM. After address is stable, local selects are generated for both the PROM and the RAM. The PROM local select produces the INH1/ signal which then removes the RAM local select and its driver enable. Because the slave RAM has been inhibited after it had already begun its cycle, the PROM XACK/ must be delayed ($t_{ACCB}$) until after the latest possible acknowledgement from the RAM ($t_{ACCA}$).

### Bus Control Exchange Operations

The bus control exchange operation (Figure 4) illustrates the relationship among the bus contention resolution signals using the parallel bus priority technique.

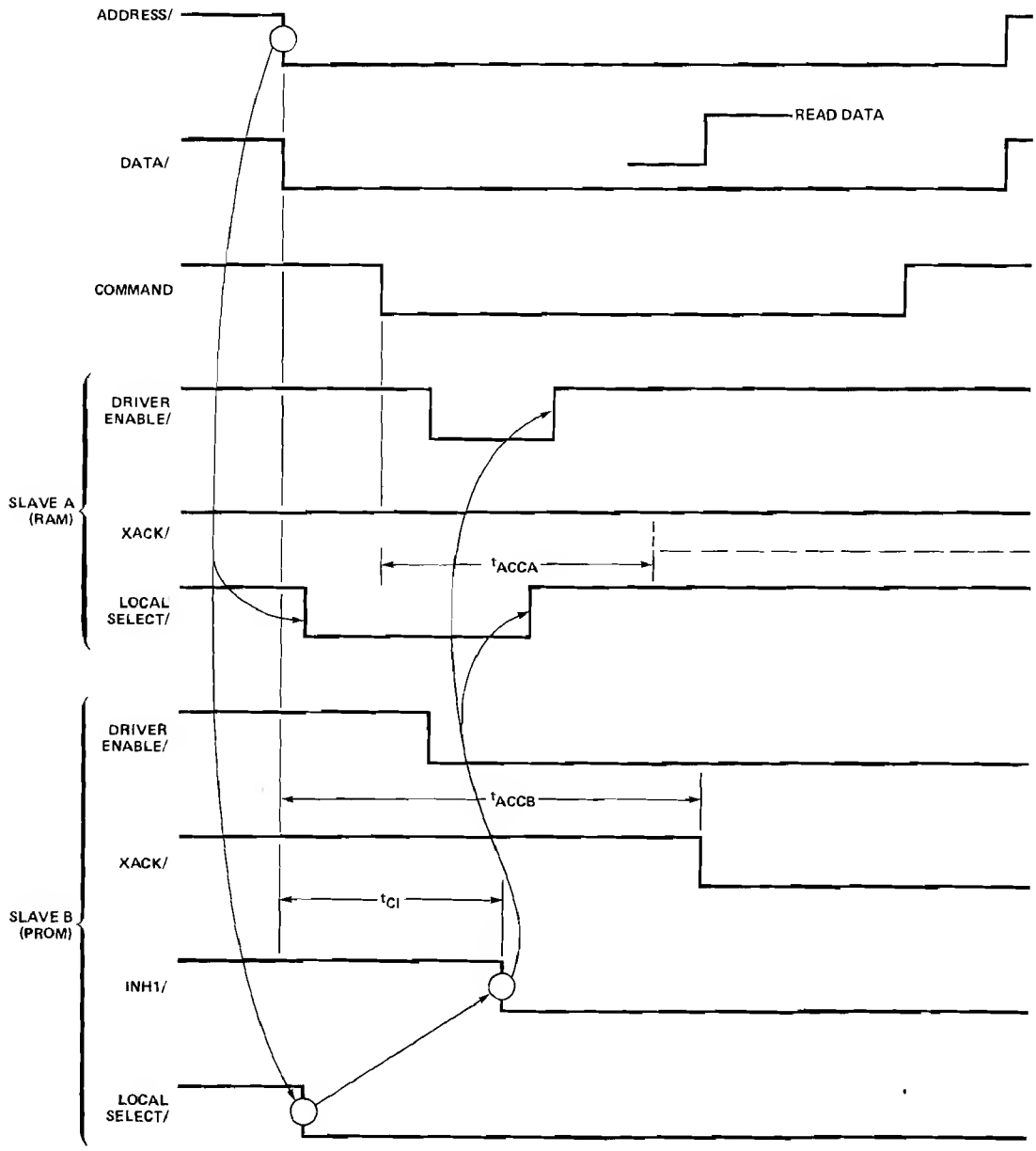



**Figure 3. Inhibit Operation**

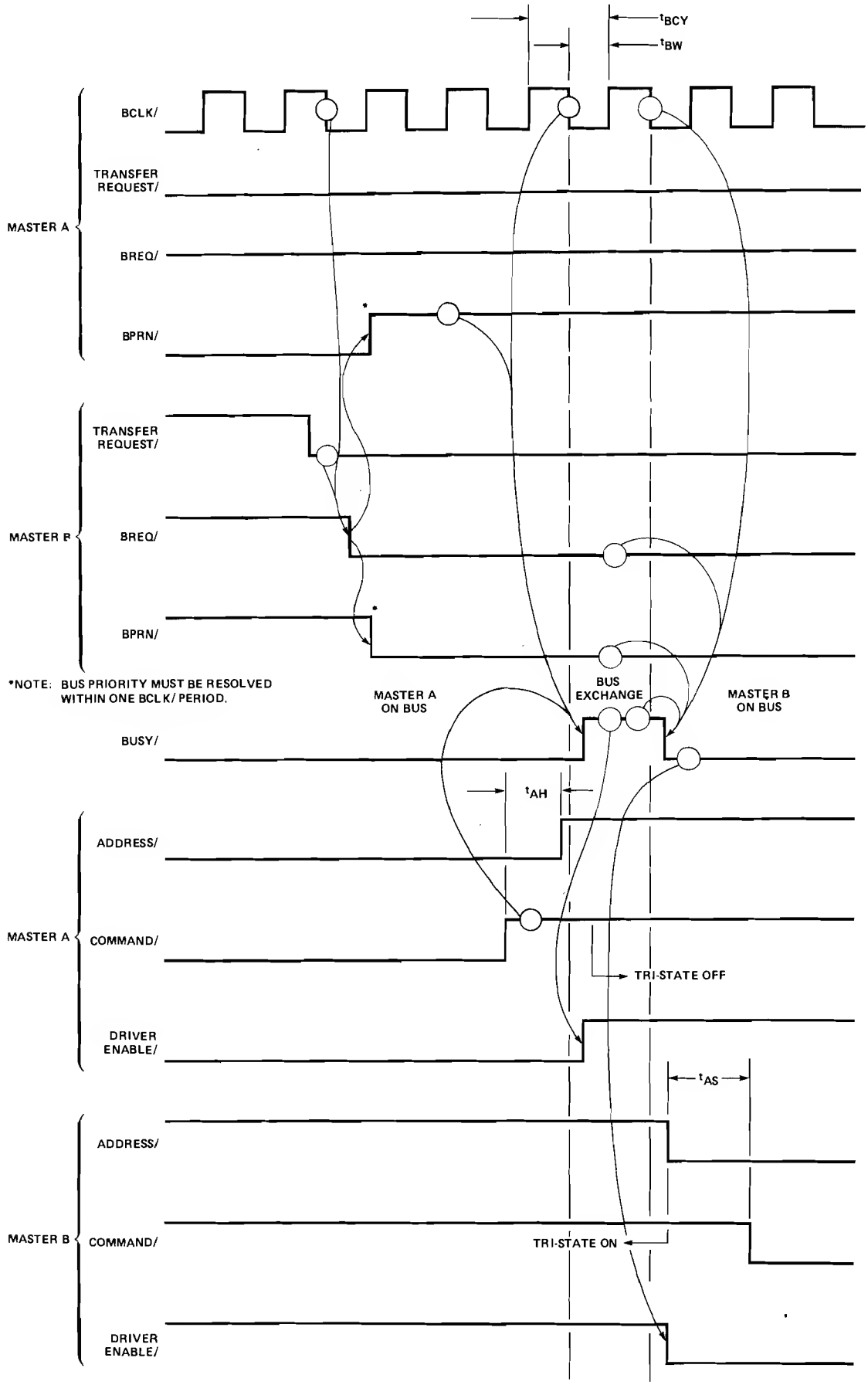



**Figure 4. Bus Control Exchange Operation**

In this example master A has been assigned a lower priority than master B. The bus exchange occurs because master B asserts a bus request during a time when master A has control of the bus.

The exchange process begins when master B requires the bus to access some resource such as an I/O or memory module. This internal transfer request is synchronized with the falling edge of BCLK/ to generate a bus BREQ/ signal. The active BPRN/ signal to master A goes inactive because of the BREQ/ from master B. When the BPRN/ signal to master A is inactive and master A has completed a command which may have been in operation, the falling edge of BCLK/ is used to synchronize BUSY/ going inactive. This allows the actual exchange to occur because control of the bus has been relinquished and another master may then assume control. During this time the drivers of master A are disabled. Master B must take control of the bus with the next falling edge of BCLK/, completing the actual bus exchange. Master B takes control by asserting BUSY/ and enabling its drivers. Thus a full BCLK/ period in addition to the synchronization of the internal transfer request is required for the bus exchange between masters and must be included in bus latency calculations.

### DC Requirements

The drive and load characteristics of the bus signals are listed in Appendix B. The physical locations of the drivers and loads, as well as the pull-up/down resistor of each bus line, are also specified. The MULTIBUS DC requirements for drive and loading are guidelines only. These guidelines are used on Intel OEM products.

## MULTIBUS INTERFACE CIRCUITS

There are three basic elements of a bus interface: address decoders, bus drivers, and control signal logic. This section discusses each of these elements in general terms. A description of a detailed implementation of a slave interface is presented in a later section of this application note.

## ADDRESS DECODING

This logic decodes the appropriate MULTIBUS address bits into RAM requests, ROM requests, or I/O selects. Care must be taken in the design of the address decode logic to ensure flexibility in the selection of base address assignments. Without this flexibility, severe restrictions may be placed upon various system configurations. Ideally, switches and jumper connections should be associated with the decode logic to permit field modification of base address assignments.

The initial step in designing the address decode portion of a MULTIBUS interface is to determine the required number of unique address locations. This decision is influenced by the fact that address decoding is usually done in two stages. The first stage decodes the base address, producing an enable for the second stage which generates the actual device selects for the user logic. A convenient implementation of this two stage decoding scheme utilizes a single decoder driven by the high order bits of the address for the first stage and a second decoder for the low order bits of the address bus. This technique forces the number of unique address locations to be a power of two, based at the address decoded by the first stage. Consider the scheme illustrated in Figure 5.

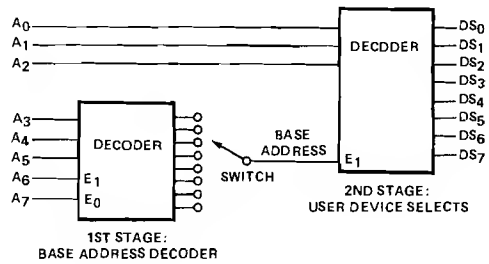



**Figure 5. Two Stage Decoding Scheme**

As shown in Figure 5, the address bits $A_7$–$A_3$ are used to produce switch selected data outputs of the first stage of decoding. A one of eight decoder has been used, with two of the address bits ($A_6$ and $A_7$) driving enable inputs. The address bits $A_2$–$A_0$ enter the second stage decoder to produce 8 user device selects when enabled by an address that corresponds to the switch-selected base address.

Address decoding must be completed before the arrival of a command. Since the command may become active within 50 ns after stable address, the decode logic should be kept simple with a minimal number of layers of logic. Furthermore, the timing is extremely critical in systems which make use of the inhibit lines.

A linear select scheme in which no decoding is performed is not recommended for the following reasons. First, the scheme offers no protection in case multiple devices are simultaneously selected. And second, the addressing within such a system is restricted by both the lack of flexibility in base address selection and by the extent of the address space occupied by such a scheme.

## BUS DRIVERS

The Intel MULTIBUS requires three-state drivers on the bidirectional data lines. For user designed logic which simply receives data from the MULTIBUS, this portion of the bus interface logic may only consist of buffers. Buffers would be required to ensure that maximum allowable bus loading is not exceeded by the user logic.

In systems where the user designed logic must place data onto the MULTIBUS, three-state drivers are required. These drivers should be enabled only when a memory read command (MRDC/) or an I/O read command (IORC/) is present and the module has been addressed.

When both the read and write functions are required, parallel bidirectional bus drivers (e.g., Intel 8216/8226) are used. A note of caution must be included for the designer who uses this type of device. A problem may arise if data hold time requirements must be satisfied for user logic following write operations. When bus commands are used to directly produce both the chip select for the bidirectional bus driver and a strobe to a latch in the user logic, removal of that signal may not provide the user's latch with adequate data hold time. Depending on the specifics of the user logic, this problem may be solved by permanently enabling the data buffer's receiver circuits.

## CONTROL SIGNAL LOGIC

The control signal logic consists of the circuits that forward the I/O and memory read/write commands to their respective destinations, provide the bus with transfer acknowledge responses, and drive the system interrupt lines.

### Bus Command Lines

The MULTIBUS information transfer protocol lines (MRDC/, MWTC/, IORC/ and IOWC/) should be buffered by devices with very high speed switching. Because the bus DC requirements specify that each board may load these lines with 2.0 mA, Schottky devices are recommended. The commands are gated with the signal indicating whether or not the base address has been decoded to generate read and write strobes for the user logic.

### Transfer/Advance Acknowledge Generation

The user interface transfer/advance acknowledge generation logic provides a transfer acknowledge response, XACK/, to notify the bus master that write data provided by the bus master has been accepted or that read data it has requested is available on the MULTIBUS. XACK/ allows the bus master to conclude its current instruction. Another signal, advanced acknowledge (AACK/), can be used in some 8080 based systems as an advance notification that requested data will be valid when the bus master is ready to use it. This early acknowledge may decrease by one the number of Wait states needed to complete a read or write operation. You should have a thorough knowledge of the 8080 (as provided in the *8080 Microcomputer System User's Manual, 98-153*) before attempting to use AACK/.

AACK/ can be used in certain applications where an early acknowledgment to the 8080 is needed to allow it to proceed to the T3 state following the current T2 or Wait state. Such applications have the following characteristics – XACK/ is generated too late for the 8080 to detect it in the current state, but

1. valid read data will be placed on the bus by the time the 8080 needs it in the current state, or
2. write data will be accepted from the bus by the time the 8080 has completed its write operation.

In either case, AACK/ is sent to the 8080 CPU-based bus master early enough in the current state (T2 or Wait) to prevent the CPU from entering a subsequent Wait state. The read or write transaction is completed during the current T2 or Wait state and the CPU moves on to T3.

It is important to note that XACK/ must be driven whether or not AACK/ is used. This requirement exists because not all bus masters will respond to AACK/.

Since XACK/ and AACK/ timing requirements depend on both the CPU of the bus master and characteristics of the user logic, a circuit is needed which will provide a range of easily modified acknowledge responses.

The transfer acknowledge signals must be driven by three-state drivers which are enabled when the bus interface is addressed and a command is present.

### Interrupt Signal Lines

The asynchronous interrupt lines must be driven by open collector devices with a minimum drive of 16 mA.

In a typical system, logic must be provided to assert and latch up an interrupt signal. The latched interrupt signal would be removed at a later time by an I/O operation such as reading the module's status.

## GENERAL PURPOSE SLAVE INTERFACE

Learning by example is often the most effective means for absorbing technical information. With this idea in mind, a detailed description of a general purpose slave interface (GPSI) has been included in this application note. The description is generally directed towards the implementation of an I/O interface. However, the GPSI can also be used as a slave memory interface by simply buffering the additional address signals and using the appropriate MULTIBUS memory commands.

The most significant aspect of the GPSI is that all the information required to actually construct the interface is contained in Appendix C. You can make use of the schematic and wire list to prototype your application.

## FUNCTIONAL/PROGRAMMING CHARACTERISTICS

This section briefly describes the organization of the GPSI from two points of view. The principal functions performed by the hardware are identified and the general data flow is illustrated. This first point of view is intended as an introduction to the detailed information provided in the next section, Theory of Operation. In the second point of view the information needed by a programmer to access the GPSI is summarized.

### Functional Description

The function of the GPSI is to provide bus interface logic which consists of those circuit elements most directly involved with communication between the bus master and the GPSI. These elements include bus address/control line receivers, bidirectional data buffer, device select decode logic, transfer acknowledge generation, and line driver circuits.

A functional block diagram of the GPSI is shown in Figure 6.

### Programming Characteristics

The GPSI addressing provides 8 unique device selects and a single line which may be used to indicate control/data. The module's base address is assigned through the use of wire wrap connections on the prototype board. Two such jumpers are part of the board's address decode circuit for system address bits ADR4/–ADR7/. They allow the selection of a base address for the GPSI on a 16-byte boundary. Address bits ADR1/–ADR3/ are decoded by other logic to provide 1 of 8 device selects for the user. A single line to implement a control/data select function is provided by ADRØ/.

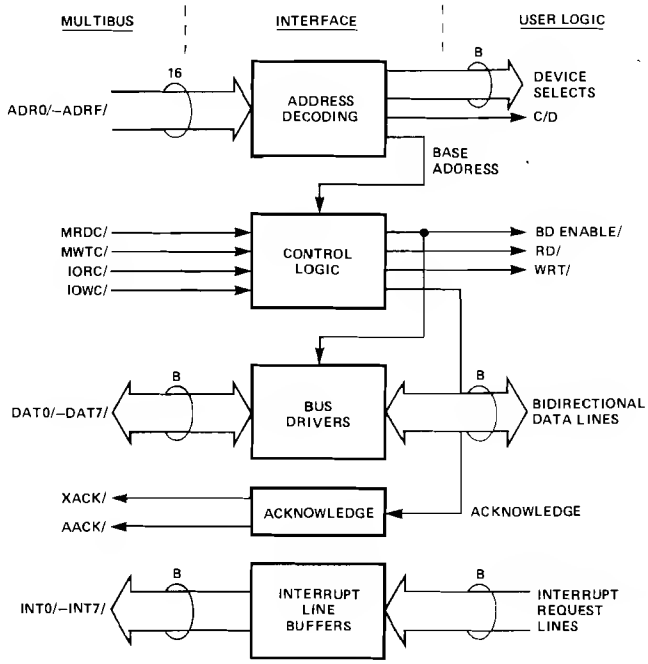



**Figure 6. GPSI Block Diagram**

Effectively, this signal is used to select one of the two 8 device address groups, yielding a total of 16 device addresses. The control/data line can also be used directly with Intel peripheral chips such as the 8251.

The GPSI may be configured to provide either direct or memory mapped I/O for program access to its devices. When direct I/O is used, the various devices are accessed by the addresses shown in Table 2.

**Table 2**

**GPSI ADDRESSING**

| DEVICE | C/D = 0 | C/D = 1 |
|---|---|---|
| 1 | X0 | X1 |
| 2 | X2 | X3 |
| 3 | X4 | X5 |
| 4 | X6 | X7 |
| 5 | X8 | X9 |
| 6 | XA | XB |
| 7 | XC | XD |
| 8 | XE | XF |

X = Any hex digit; assigned by jumper; X is the same for all GPSI devices.

When the GPSI is configured for memory mapped I/O, the low order 8 bits of the 16-bit address are identical to those shown in Table 2 for direct I/O. However, the upper 8 bits of the address must be all ones. Thus, the addressable devices occupy space within the upper 256 bytes of memory, FFØØ Hex to FFFF Hex.

## THEORY OF OPERATION

In the preceding section each of the GPSI functional blocks was identified and briefly defined. This section explains how these functions are implemented. For detailed circuit information, refer to the GPSI schematic in Appendix C. The schematic is on a foldout page so that you can relate the following text to the schematic.

The GPSI contains those logic elements that participate directly in the following types of MULTIBUS activity.

1. Bus address, control, and data buffering
2. Bus address decoding
3. Bus control signal propagation
4. Advance/Transfer acknowledge generation
5. Interrupt signal buffers.

The five groups of logic responsible for these tasks are described in the following paragraphs.

### Bus Address, Control, and Data Buffers

Only one bit of the bus address is buffered and passed directly onto the user logic. The rest of the address bits are used to drive decoders. ADRØ/ is buffered by a 74LS02 ($A_{13}$). The control signal buffer circuit consists of a 74S32 ($A_1$) and a 74S10 ($A_2$) for the memory and I/O read/write commands. These circuits are used to provide very high switching speed.

The data buffers are formed by two Intel 8226 inverting bidirectional driver/receiver chips ($A_{10}$ and $A_{11}$). The system data bus is connected to the device's DB pins. The DO and DI pins of each chip can be connected to the user logic, providing either an independent input and output bus or a bidirectional bus.

Directional control (DIEN/) for the 8226's is exercised by the I/O read command (IORC/) or the memory read command (MRDC/) in situations where memory mapped I/O is used. If the read command is asserted by the bus master and the module's base address is present, the data buffer's receiver circuits are enabled.

The chip select (CS/) for the data buffer is enabled when a command is gated onto the board.

### Bus Address Decoding

The bus address decoding logic decodes the appropriate address bits into device selects. When memory mapped I/O is used, all ones on the high order 8 bits of the address are decoded. The GPSI logic also produces an enable for the read/write command decode logic and the MULTIBUS inhibit signals.

The base address is decoded by an Intel 8205 one of eight binary decoder ($A_8$). This device is enabled by either ADR7/ or ADR7, as determined by the wire-wrap connections. When enabled, $A_8$ decodes address bits ADR4/, ADR5/, and ADR6/ into one of eight outputs. The base address enable (BASE ADR/) may be taken from any one of the eight $A_8$ outputs.

When the ADR4/ through ADR7/ bits correspond to the selected base address, an enable is provided by $A_8$ to a device select generator ($A_9$) and the read/write command gates ($A_1$).

The device select generator consists of an Intel 8205 decoder ($A_9$) that is enabled by the base address. When enabled, $A_9$ decodes address bits ADR1/, ADR2/, and ADR3/ into one of eight device select outputs.

When memory mapped I/O is used, the high order 8 bits of the address bus are also decoded. The address bits ADR8/ through ADRF/ are used as inputs to a 74LS27 ($A_7$). The outputs of $A_7$ are ANDed by a 74S10 ($A_2$), producing an active low output only when ADR8/–ADRF/ are all active. This output signal, MMIO/, is used to generate optional inhibit signals as well as to enable the memory read and write commands when a connection is made between $A_{2-8}$ and $A_{4-3}$.

The MMIO/ signal is inverted twice, first by a 74S04 ($A_{14}$) and then by 7406 open collector drivers ($A_6$). At that point the signal can be connected to the system INH1/ and/or INH2/ bus signal lines.

The only situation in which the inhibit lines are required is if there is ROM or RAM in the system which physically occupies the upper 256 bytes of memory. When this is the case, you may choose to disable the memory mapped I/O capability and use direct I/O. Otherwise, you must select the proper inhibit connection to allow use of the memory mapped I/O. INH1/ is used to inhibit RAM, while INH2/ inhibits ROM.

With a worst case delay of 53 nanoseconds, the decode circuit that produces the inhibit signals meets the bus AC requirement for inhibit delay ($t_{CI}$). However, the acknowledge of the inhibiting slave ($t_{ACCB}$) is a much more difficult specification to satisfy. The difficulty arises because the latest possible acknowledgement from the inhibited slave memory ($t_{ACCA}$) must be known to ensure an adequate $t_{ACCB}$. In the worst case $t_{ACCB}$ must be at least 1.5 microseconds. The acknowledge delay circuit, which will be described later, provides for a maximum of approximately 800 nsec. In situa-

tions where a 1.5 μsec $t_{ACCB}$ is required, the clock frequency of the delay circuit must be halved or another device added to extend the selectable delay to 1.5 μsec. In this situation it may well be a better choice to disable the memory mapped I/O in favor of the simple direct I/O technique.

If the GPSI module is to reside in an Intel Microcomputer Development System (Intellec) the memory mapped I/O capability must be disabled. This restriction exists because the Intellec has ROM program memory which occupies the entire memory mapped I/O region (FFØØH to FFFFH) and must not be overridden by the GPSI.

### Bus Control Signal Propagation

A pair of 74S32 OR gates ($A_1$) buffer the MRDC/ (memory read command) and MWTC/ (memory write command) inputs from the MULTIBUS. These gates are enabled by the MMIO/ (memory mapped I/O) signal from the high order address decoder.

The gated and buffered memory read and write commands are then each ORed and buffered with their respective I/O read and write commands by a pair of 74S10 NAND gates ($A_2$). The output of these gates are active high read and write commands.

These commands are passed on to the advance/transfer acknowledge generator via NOR gate $A_{13}$. The output of $A_{13}$ is designated CMD/. CMD/ is enabled by the decoded base address at OR gate $A_1$ to produce the board enable. This signal, BD ENABLE/, controls the three-state gates that drive AACK/ and XACK/ onto the MULTIBUS. BD ENABLE/ also controls the chip selects for the data bus buffers.

The output of the I/O and memory write buffer is inverted with a 74S04 ($A_{14}$) and forwarded as WRT/ to the user logic. This internal write enable should be qualified at each of these destinations by the appropriate device select.

The output of the I/O and memory read buffer is inverted and then enabled by the decoded base address at $A_1$. The resulting internal read enable, RD/, is applied to the user logic and to the direction control (DIEN) on the bidirectional bus driver chips ($A_{10}$ and $A_{11}$).

### Advance/Transfer Acknowledge Generation

The advance/transfer acknowledge generation logic provides a transfer acknowledge response, XACK/, to notify the bus master that data has either been accepted from the MULTIBUS (during a write operation) or placed on the MULTIBUS (during a read operation). An advance acknowledge response, AACK/, is also provided for use in certain 8080-based systems, where it can decrease by one the number of Wait states needed to complete a read or write operation.

Both acknowledge responses are generated by $A_{12}$, an 8-bit serial in, parallel out shift register. When enabled by CMD, $A_{12}$ shifts CCLK/ pulses. This produces a sequence of high true pulses at $A_{12}$'s Q outputs. The outputs occur at approximately 100 ns intervals.

The appropriate Q outputs are selected by wire-wrap connections to the inputs of a pair of three-state gates ($A_3$). These gates drive the XACK/ and AACK/ outputs onto the MULTIBUS when enabled by BD ENABLE/.

As mentioned in the previous discussion on inhibit operations, the maximum of about 800 ns delay provided by $A_{12}$ may not be adequate. This can be extended by either using a flip-flop to pre-divide CCLK/ or by adding a second shift register in series with $A_{12}$. Although both techniques double the range, the first cuts the resolution in half.

### Interrupt Signal Buffers

The GPSI only provides buffering for the bus interrupt signal lines. Two 7406 open collector drivers ($A_5$ and $A_6$) are used for this function.

The MULTIBUS interrupt signals should be driven with levels rather than pulses, unless the bus master has an edge triggered interrupt controller. The user's logic must latch and hold the interrupt signal until serviced by the bus master.

## USER SELECTABLE OPTIONS

In this section, each of the options available to the user is reviewed and the specific information required to implement the desired characteristic is summarized.

### Base Address Selection

The GPSI's base address is selected by wire-wrap connections from one of the output pins of $A_8$ to an enable input ($E_2$) of $A_9$. Table 3 identifies the base address that is implemented for each jumper combination.

Table 3

BASE ADDRESS SELECTION

| FROM | TO | FROM | TO | BASE ADDR | FROM | TO | FROM | TO | BASE ADDR |
|---|---|---|---|---|---|---|---|---|---|
| P1-52 | A8-6 | A8-7 | A9-5 | 00 | P1-52 | A8-5 | A8-7 | A9-5 | 80 |
| GND | A8-5 | A8-9 | A9-5 | 10 | A4-1 | A8-6 | A8-9 | A9-5 | 90 |
| | | A8-10 | A9-5 | 20 | | | A8-10 | A9-5 | A0 |
| | | A8-11 | A9-5 | 30 | | | A8-11 | A9-5 | B0 |
| | | A8-12 | A9-5 | 40 | | | A8-12 | A9-5 | C0 |
| | | A8-13 | A9-5 | 50 | | | A8-13 | A9-5 | D0 |
| | | A8-14 | A9-5 | 60 | | | A8-14 | A9-5 | E0 |
| | | A8-15 | A9-5 | 70 | | | A8-15 | A9-5 | F0 |

### Advance/Transfer Acknowledge Timing

The GPSI's advance acknowledge and transfer acknowledge response timing is selected in approximately 100 ns increments by wire-wrap connections at the outputs of $A_{12}$. Table 4 shows the range of response timing for each possible connection in terms of CCLK/ periods. This range occurs because of the skew introduced into the acknowledge circuit by the use of CCLK/ to drive $A_{12}$. Actual time values for these periods depend, of course, on the frequency of CCLK/. For the SBC 80/10 or 80/20 bus masters, CCLK/ is 9.216 MHz, which provides a clock period of 108.5 nanoseconds.

Table 4

ADVANCE/TRANSFER ACKNOWLEDGE TIMING

| PIN CONNECTIONS | | | | DELAY FROM RECEIPT OF CMD TO ACK GENERATION | |
|---|---|---|---|---|---|
| AACK | | XACK | | | |
| FROM: | TO: | FROM: | TO: | | |
| A4-4 | A3-12 | A4-4 | A3-14 | Immediate | |
| A12-3 | A3-12 | A12-3 | A3-14 | 0 to 1 | CCLK/ Periods |
| A12-4 | A3-12 | A12-4 | A3-14 | 1 to 2 | |
| A12-5 | A3-12 | A12-5 | A3-14 | 2 to 3 | |
| A12-6 | A3-12 | A12-6 | A3-14 | 3 to 4 | |
| A12-10 | A3-12 | A12-10 | A3-14 | 4 to 5 | |
| A12-11 | A3-12 | A12-11 | A3-14 | 5 to 6 | |
| A12-12 | A3-12 | A12-12 | A3-14 | 6 to 7 | |
| A12-13 | A3-12 | A12-13 | A3-14 | 7 to 8 | CCLK/ Periods |

## PROTOTYPING APPLICATIONS

The GPSI should be well suited for most prototyping applications by constructing the interface on a SBC 905 Universal Prototype Board. A complete wire list is provided in Appendix C to further simplify the task. The complete general purpose slave interface requires 14 IC's and can best be laid out by placement from left to right, $A_1$–$A_{14}$, across the bottom of the SBC 905 (Figure 7). Using the GPSI constructed on an SBC 905, you have the capacity for an additional 80 16-pin locations for wire-wrap sockets or the equivalent mix of 14, 16, 18, 22, 24, 28 or 40-pin sockets.

## SUMMARY

This application note has shown the structure of the Intel MULTIBUS. The structure supports a wide range of system modules from the Intel OEM Computer Product Line that can be extended with the addition of user designed modules. Because the user designed modules are no doubt unique to particular applications, a goal of this application note has been to describe in detail the singular common element – the bus interface. Material has also been presented to assist the systems designer in understanding the bus functions so that successful systems integration can be achieved.

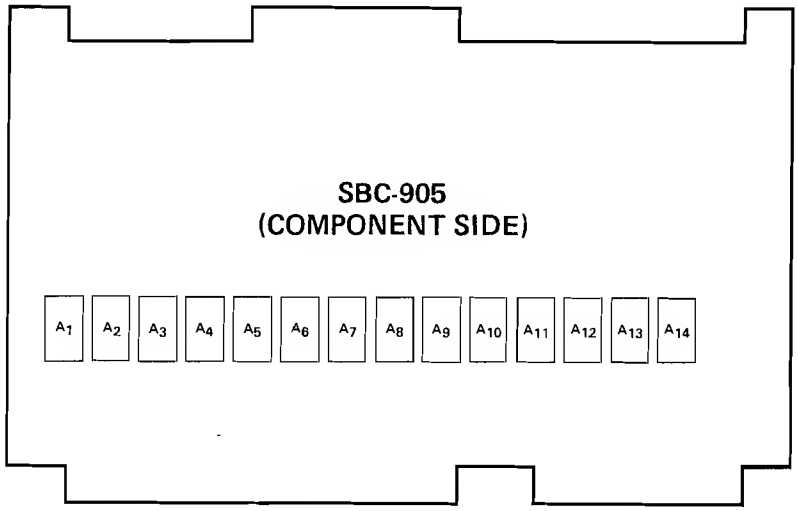



**Figure 7. Prototype Board Layout**

# APPENDIX A
## MULTIBUS PIN ASSIGNMENT

| | (COMPONENT SIDE) | | | (CIRCUIT SIDE) | | |
|---|---|---|---|---|---|---|
| | PIN | MNEMONIC | DESCRIPTION | PIN | MNEMONIC | DESCRIPTION |
| Power Supplies | 1 | GND | Signal GND | 2 | GND | Signal GND |
| | 3 | +5 | +5 VDC | 4 | +5 | +5 VDC |
| | 5 | +5 | +5 VDC | 6 | +5 | +5 VDC |
| | 7 | +12 | +12 VDC | 8 | +12 | +12 VDC |
| | 9 | -5 | -5 VDC | 10 | -5 | -5 VDC |
| | 11 | GND | Signal GND | 12 | GND | Signal GND |
| Bus Controls | 13 | BCLK/ | Bus Clock | 14 | INIT/ | Initialize |
| | 15 | BPRN/ | Bus Priority In | 16 | BPRO/ | Bus Priority Out |
| | 17 | BUSY/ | Bus Busy | 18 | BREQ/ | Bus Request |
| | 19 | MRDC/ | Memory Read Command | 20 | MWTC/ | Memory Write Command |
| | 21 | IORC/ | I/O Read Command | 22 | IOWC/ | I/O Write Command |
| | 23 | XACK/ | XFER Acknowledge | 24 | INH1/ | Inhibit 1 Disable RAM |
| | 25 | AACK/ | Special Acknowledge | 26 | INH2/ | Inhibit 2 Disable PROM or ROM |
| | 27 | | Reserved | 28 | | Reserved |
| | 29 | | Reserved | 30 | | Reserved |
| | 31 | CCLK/ | Constant Clk | 32 | | Reserved |
| | 33 | | Reserved | 34 | | Reserved |
| Interrupts | 35 | INT6/ | Parallel Interrupt Requests | 36 | INT7/ | Parallel Interrupt Requests |
| | 37 | INT4/ | | 38 | INT5/ | |
| | 39 | INT2/ | | 40 | INT3/ | |
| | 41 | INT0/ | | 42 | INT1/ | |
| Address | 43 | ADRE/ | Address Bus | 44 | ADRF/ | Address Bus |
| | 45 | ADRC/ | | 46 | ADRD/ | |
| | 47 | ADRA/ | | 48 | ADRB/ | |
| | 49 | ADR8/ | | 50 | ADR9/ | |
| | 51 | ADR6/ | | 52 | ADR7/ | |
| | 53 | ADR4/ | | 54 | ADR5/ | |
| | 55 | ADR2/ | | 56 | ADR3/ | |
| | 57 | ADR0/ | | 58 | ADR1/ | |
| Data | 59 | DATE/ | Data Bus | 60 | DATF/ | Data Bus |
| | 61 | DATC/ | | 62 | DATD/ | |
| | 63 | DATA/ | | 64 | DATB/ | |
| | 65 | DAT8/ | | 66 | DAT9/ | |
| | 67 | DAT6/ | | 68 | DAT7/ | |
| | 69 | DAT4/ | | 70 | DAT5/ | |
| | 71 | DAT2/ | | 72 | DAT3/ | |
| | 73 | DAT0/ | | 74 | DAT1/ | |
| Power Supplies | 75 | GND | Signal GND | 76 | GND | Signal GND |
| | 77 | -10* | -10 VDC | 78 | -10* | -10 VDC |
| | 79 | -12 | -12 VDC | 80 | -12 | -12 VDC |
| | 81 | +5 | +5 VDC | 82 | +5 | +5 VDC |
| | 83 | +5 | +5 VDC | 84 | +5 | +5 VDC |
| | 85 | GND | Signal GND | 86 | GND | Signal GND |

*For MDS 800 compatibility.

# APPENDIX B

## MULTIBUS DC REQUIREMENTS

| BUS SIGNALS | DRIVER | | LOAD PER BOARD | | PULL-UP/DOWN RESISTOR |
|---|---|---|---|---|---|
| | LOCATION | DRIVE (Min) | LOCATION | SOURCING (Max) | |
| INIT/ | Master | TTL, 32 mA | All | 1.8 mA | None |
| BCLK/, CCLK/ | Master | TTL, 48 mA | Master | 2.0 mA | 220/330Ω termination on Motherboard |
| BREQ/ | Master | TTL, 16 mA | | 2.0 mA | 1 kΩ pull-up on Motherboard |
| BPRN/ | Master | TTL, 16 mA | Master | 2.0 mA | None |
| BPRO/ | Master | TTL, 32 mA | Master | 2.0 mA | None |
| BUSY/ | Master | OC, 20 mA | Master | 2.0 mA | 1.0 kΩ pull-up |
| MRDC/, MWTC/ | Master | TRI, 32 mA | Slave | 2.0 mA | 1.1 kΩ pull-up |
| IORC/, IOWC/ | Master | TRI, 32 mA | I/O Board | 2.0 mA | 1.1 kΩ pull-up |
| XACK/, AACK/ | Slave | TRI, 16 mA | Master | 2.0 mA | 510 Ω pull-up |
| DATF/–DATØ/ | Master | TRI, 15 mA | Slave | 0.5 mA | 2.2 kΩ pull-up |
| ADRF/–ADRØ/ | Master | TRI, 15 mA | Slave | 0.5 mA | 2.2 kΩ pull-up |
| INH1/, INH2/ | All | OC, 16 mA | RAM, PROM, Memory Mapped I/O | 2.0 mA | 1 kΩ pull-up |
| INT7/–INTØ/ | All | OC, 16 mA | Master | 2.0 mA | 1 kΩ pull-up |

**NOTES:** 1. Input voltage levels: High 2.4V to 5.0V
Low 0.0V to 0.8V

2. Output voltage level: High 2.0V to 5.25V
Low 0.0V to 0.45V

OC – open collector
TTL – totem-pole output
TRI – three-state

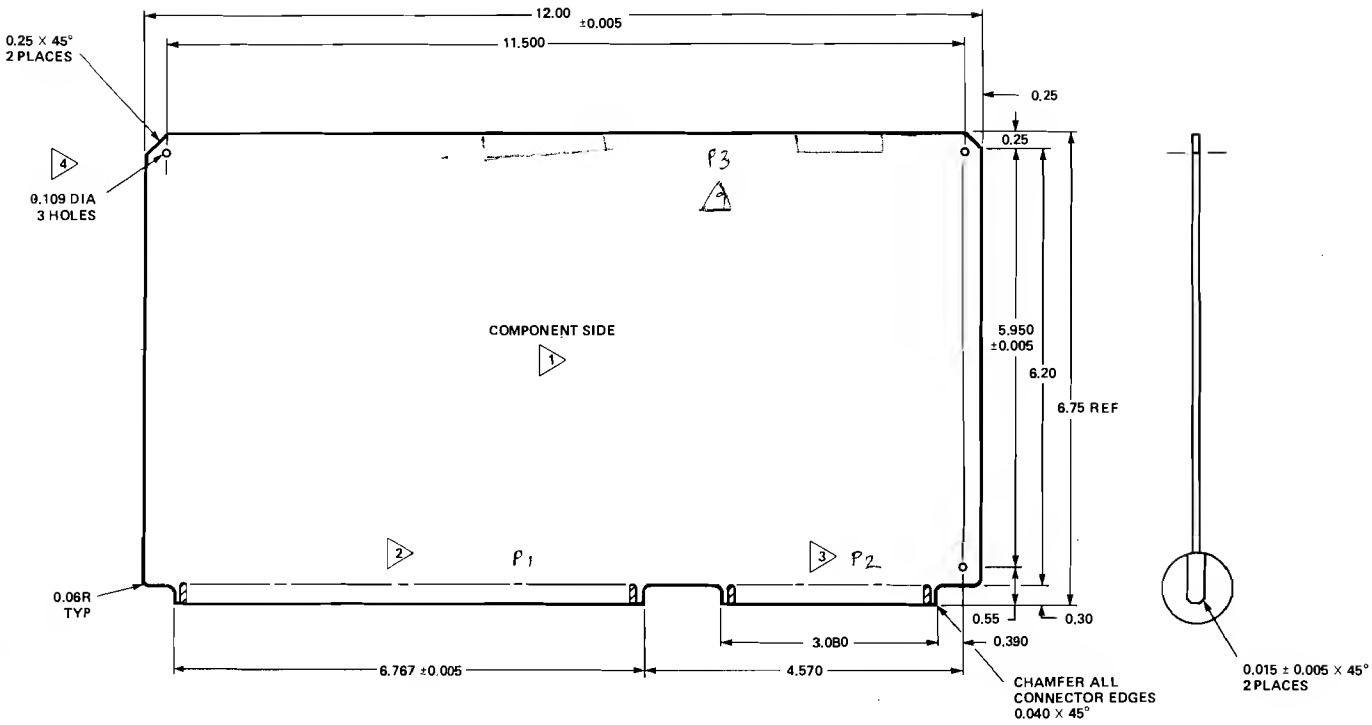
3. Leakage current of an input ≤40 μA
Leakage current of an output ≤100 μA
4. Maximum number of Master devices = 16 using parallel priority network.
5. Maximum bus capacitance is 300 pF.

## APPENDIX C
## GPSI INTERFACE SCHEMATIC AND WIRE LIST

(FOLDOUT)

# APPENDIX D

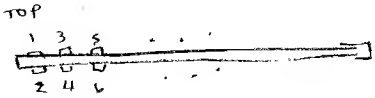
## MECHANICAL SPECIFICATIONS




NOTES:

1. BOARD THICKNESS: 0.062
2. MULTIBUS CONNECTOR: 86-PIN, 0.156 SPACING
   CDC VFB01E43D00A1
   VIKING 2VH43/1ANE5
3. AUXILIARY CONNECTOR: 60-PIN, 0.100 SPACING
   CDC VPB01B30D00A1
   TI H311130
   AMP PE5-14559
4. EJECTOR TYPE: SCANBE #S203
5. BUS DRIVERS AND RECEIVERS SHOULD BE LOCATED AS CLOSE AS POSSIBLE TO THEIR RESPECTIVE MULTIBUS PIN CONNECTIONS
6. BOARD SPACING: 0.6
7. COMPONENT HEIGHT: 0.435
8. CLEARANCE ON CONDUCTOR NEAR EDGES: 0.050
9. CONNECTOR P3 50 MIL SPACING

ALL CONNECTORS



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